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714	718	Subclass
ISSUE CLASSIFICATION		

PATENT NUMBER

U.S. REISSUE Patent Application

O.I.P.E.	O.G. PUBLICATION DATE	REISSUE PATENT DATE
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APPLICATION NO. 09/871978	CONT/PRIOR D	CLASS 714	SUBCLASS 718	ART UNIT 2133	EXAMINER Ton 7367
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TITLE . . . APPLICANTS

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Semiconductor integrated circuit comprising synchronous DRAM core and logic circuit integrated into a single chip and method of testing the synchronous DRAM core

PTO-2040
12/99

☐ SURRENDER OF ORIGINAL PATENT _____ (Exr. Initials) ORIGINAL PATENT NUMBER _____

ISSUING CLASSIFICATION

ORIGINAL				CROSS REFERENCE(S)									
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)								
714		718											
INTERNATIONAL CLASSIFICATION													
G	0	6	F	11/00									

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	<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.		NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____	_____ (Assistant Examiner) (Date)		ISSUE FEE	
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FINAL SPRE REVIEW _____ (INITIALS)	_____ (Primary Examiner) (Date) 3/19/04		ISSUE BATCH NUMBER	
	_____ (Legal Instruments Examiner) (Date)			

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